AMENDMENTS TO THE CLAIMS

1. A wireless peak suppression and pre-distortion circuit for use with multi-carrier power amplifiers in a wireless communication system to enhance linearity and performance of the amplifier, in wireless cellular, PCS, wireless LAN, line of sight microwave, military, or satellite communication systems, the peak suppression and pre-distortion circuit comprising:

two multi-carrier receivers one for the peak suppression and pre-distortion main IF or RF signal input and one for amplifier feedback input; wherein when the main signal is baseband then the main multi-carrier receiver is bypassed;

a digital signal processing block to peak suppress and pre-distort the main multi-carrier input signal using lookup tables;

a digital signal processing block to use the main multi-carrier input signal and amplifier feedback multi-carrier input to adaptively update a pre-distortion lookup table;

a digital signal processing block to use the input and the output of the peak suppression to produce the phase rotation lookup table;

a digital signal processing block to evaluate a delay between the main multi-carrier signal and an amplifier multi-carrier feedback signal and adjust a main signal delay before being used by a lookup table adaptation algorithm; wherein the algorithm will continuously adjust the delay during the operation;

a digital signal processing block to evaluate the gain between a main multi-carrier signal and an amplifier multi-carrier feedback signal and adjust both signal's gain before being used by a lookup table adaptation algorithm; wherein the algorithm will continuously adjust the gain during the operation;

adigital signal processing block to accurately evaluate the delay between a main multi-carrier signal and an amplifier multi-carrier feedback signal by changing the

coefficient of a decimation filter used in the path of amplifier feedback signal to produce T/k accuracy;

a multi-carrier transmitter block that prepare a peak suppressed and pre-distorted main multi-carrier signal for delivery to a multi-carrier power amplifier.

2. The peak suppression and pre-distortion circuit according to claim 1, wherein main multi-carrier input signal from the wireless transmitter is sampled using sub-harmonic sampling technique at the input frequency or at an intermediate frequency.

3. The peak suppression and pre-distortion circuit according to claim 1, wherein main multi-carrier input signal from the wireless transmitter is sampled using sub-harmonic sampling technique at the input frequency or at an intermediate frequency and the digitized main multi-carrier input signal is down converted digitally and decimated to the appropriate number of samples per symbol for further digital signal processing.

4. The peak suppression and pre-distortion circuit according to claim 1, wherein main multi-carrier input signal from the wireless transmitter is baseband and is sampled using Nyquist sampling technique and interpolated to produce the baseband multi-carrier signal with appropriate number of samples per symbol.

5. The peak suppression and pre-distortion circuit according to claim 1, wherein main input signals from the wireless transmitter are in bit domain and the bit domain baseband signals are up converted, combined and interpolated to produce the digital multi-carrier baseband signal with appropriate number of sample per symbol.

6. The peak suppression and pre-distortion circuit according to claim 1, wherein feedback multi-carrier input signal from the wireless multi-carrier power amplifier is sampled using sub-harmonic sampling technique at the input frequency or at an intermediate frequency.

7. The peak suppression and pre-distortion circuit according to claim 1, wherein feedback multi-carrier input signal from the wireless multi-carrier power amplifier is sampled using sub-harmonic sampling technique at the input frequency or at an intermediate frequency and the digitized feedback input signal is down converted digitally and decimated to the appropriate number of samples per symbol for further digital signal processing.

8. The peak suppression and pre-distortion circuit according to claim 1, wherein the digital multi-carrier main baseband signal is converted to single channel baseband signals by digital down conversion. The individual baseband signals are phase rotated using the phase from phase rotation lookup table, then filtered and up converted back to their original baseband frequency before all individual baseband signals being combined again to produce the multi-carrier peak suppressed baseband signal.

9. The peak suppression and pre-distortion circuit according to claim 1, wherein the peak suppressed, and pre-distorted main signal using a lookup table is digitally up converted and converted to analog domain at an intermediate frequency or the output frequency.

10. The peak suppression and pre-distortion circuit according to claim 1, wherein the digitized main signal and feedback signal are used to adaptively update the pre-distortion lookup table, wherein the main signal samples are delayed to match the samples from the amplifier feedback input before being used by lookup table adaptation algorithm, wherein the man signal samples and the amplifier feedback signal samples are gain controlled before being used by the lookup table adaptation algorithm.

11. The peak suppression and pre-distortion circuit according to claim 1, wherein the peak suppression phase rotation lookup table is created using the input and the output from the peak suppression block during the calibration.

12. The peak suppression and pre-distortion circuit according to claim 1, wherein feedback input signal from the wireless power amplifier is sampled using sub-harmonic sampling technique at the input frequency or at an intermediate

frequency and the digitized feedback input signal is down converted digitally, decimated down to the appropriate number of samples per symbol with a sampling phase to allow phase alignment (in T/k steps) with the main input signal for further digital signal processing by the adaptation algorithm.

13. The peak suppression and pre-distortion circuit according to claim 1, wherein main input signal and digitized feedback input signal are aligned in amplitude by automatic gain control operations prior to further processing by the lookup table adaptive algorithm which updates the pre-distortion lookup table.

14. The peak suppression and pre-distortion circuit according to claim 1, wherein the delay described in claim 1 is measured by initially generating a digital signal with high autocorrelation property, such as a pseudo random sequence used by the main signal path, and correlation of this sequence with the amplifier output feedback signal by delay adjustment algorithm. The correlation window is incremented by adjusting the sampling phase in decimation block in the path of the amplifier output feedback signal in T/k steps by changing the coefficients of the decimation filter in the amplifier output feedback signal path, and by incrementing the delay of main input signal used by the delay adjustment algorithm by integer sample unit delays.

15. Canceled

16. The peak suppression and pre-distortion circuit according to claim 1, wherein the digital signal processing block can be implemented in programmable logic, FPGA, Gate Array, ASIC, and DSP processor.